# SE-CSA BASED IN-D SG DISTURB FREE VOLATILE STATIC MEMORY USING FIN-FET WITH STEEP SUBTHRESHOLD SLEEP

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**K. Shyam,** Research Scholar, Department of ECE, Sathyabama Institute of Science and Technology, (Deemed to be University) Chennai 600119, Tamil Nadu, India and **V. Vijayakumar*,** Associate Professor, Department of ECE, Sathyabama Institute of Science and Technology, (Deemed to be University) Chennai 600119, Tamil Nadu, India

*Corresponding Author: V. Vijayakumar (Email): vijayakumar.ece@sathyabama.ac.in

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**SUMMARY**

FinFET, or Fin Field-Effect Transistor, is a type of transistor used in modern semiconductor devices to overcome the limitations of traditional planar transistors as scaling continues in the nanometer range. Characterized by a three-dimensional structure, the FinFET features a "fin" shape that extends vertically from the substrate, allowing for better electrostatic control over the channel and reduced leakage currents. This design enhances performance, improves switching speed, and allows for lower power consumption compared to conventional transistors. This paper presents a novel approach to static random-access memory (SRAM) design utilizing Shorted Gate Fin-FET (SG-Fin-FET) and Independent Gate Fin-FET (IG-Fin-FET) technologies at a 7-nm process node. The proposed 8T SRAM cell architecture, which excludes read and write transistors, effectively addresses the limitations of traditional SRAM configurations by decoupling the read and write operations. This decoupling enhances the Static Noise Margin (SNM), which is measured to be approximately **0.15 V**, and significantly improves the Power Delay Product (PDP), achieving a reduction of **40%** compared to conventional SRAM designs. The Input Dependent (INDEP) technique employed reduces leakage power dissipation by nearly **50%**, thereby enhancing overall energy efficiency. Simulation results indicate a notable improvement in write capability, with a write margin of **0.2 V**. The segmented array design allows for larger memory arrays without sacrificing performance, supporting up to **1 MB** of data storage while maintaining an area efficiency of **0.35 µm²** per cell. The proposed methodology demonstrates superior flexibility in optimizing read and write functionalities, resulting in improved performance metrics suitable for high-density memory applications. The results affirm the viability of using SG-Fin-FET and IG-Fin-FET technologies for next-generation SRAM cells, offering significant advancements in both power efficiency and operational performance.

**KEY WORDS:** Short gate, Single ended current sense amplifier, Static noise margin, Input dependent, double gate, Delay, Write and read power, Leakage power.

## 1. INTRODUCTION

FinFET technology is distinctly superior to the conventional planar technology in handling issues that are realized as planar transistor scales down to the new nodes. FinFETsor Fin Field-Effect Transistors have a thin vertical silicon fin in the strip located between the source and drain [1]. This 3D structure can provide a larger electrostatic control of the channel, which reduce leakage current and enhance switching performance. For FinFETs, the gate wraps around three sides of the fin, thus giving better control to the channel and thus FinFETs can deliver better performance than planar transistors, require less power, and experience less short-channel effects [2]. This makes FinFETs critical in complicated semiconductors devices especially those that propel high speed and energy efficient ones such as mobile processors, memory chips and high performance computing [3].

FinFET static memory capitalizes on the unique attributes of FinFET to improve the prospects of static memory technologies like the SRAM [4]. Compared with traditonal transistor-based memory in planar structure, leakage currents and power dissipation become critical issues when transistors continue shrinking. Nevertheless, FinFET structure with gate enclosing the silicon fin provides a better control of the channel and results in lower leakage currents and improved power usage [5]. The end result is that FinFET static memory is much more stable and has lower power consumption in the active as well as in a state of inactivity. Moreover, the remarkably steep subthreshold slope of FinFETs results in faster signal transition and superior performance that is well suited in application such as memory, where speed, power consumption, and low disturbance level is the high [6]. Thus, FinFET Static memory is gaining wide acceptance for use in contemporary high-performance computer

systems and electronic devices mobile technology, and energy efficient systems [7–9].

A FinFET SRAM comprises units of a Static Random Access Memory that takes advantages of FinFET technology to overcome problems observed in the Planar transistor based SRAM [10–12]. These parameters are rather critical in an SRAM cell as are stability, speed and power consumption. The lack of overlap of the gate in FinFETs around the fin creates a better electrostatic control on the channel; therefore, the leakage current minimizes while the switching time improves. This lead to reduced standby power consumption, enhanced data retention, and immunity to soft error respectively [13–16]. In addition, the subthreshold slope of the FinFETs rises at a steeper angle, which makes it possible to have SRAM cells that use less power while giving high performance at high switching speed [17–20]. This makes FinFET-based SRAM cells suitable for today's low voltage applications including mobile application processors, cache memories used in high-performance computing equipment and energy-constrained systems. This innovative technology also provides better stability for read/write characteristics that are critical at down-scaled geometries of SRAM cells in future technologies [21].

A FinFET SRAM cell provides a functional CMOS SRAM cell that leverages the benefits of FinFET technology while foregoing the challenges that the conventional planar transistor based SRAM cell presents [22]. Stability, speed, and power are thought to be very important issues in an SRAM cell. The deployment of FinFET that forms three-dimensional structures around the fin and the gate control over the channel make FinFET ultralow-power devices with significantly low leakage current, low power dissipation, high switching efficiency, and better voltage scalability [23]. This leads to reduced standby power, enhanced data retention capability and diminished soft error vulnerability. With fin shaped gate control of FinFETs also results in a higher subthreshold slope that lets the SRAM cells switch on and off at a faster rate and consume, at the same time, lower power [24]. This makes FinFET based SRAM cells suitable for various modern low power application as it includes mobile processors, cache memory in high computing, and more energy efficient systems. It also improves the cell stability of read and/or write with the FinFET technology for proper efficiency of the memory at smaller geometries, a key advantage in scaling SRAM cells for future technologies [25].

Every transistor in FinFET architecture has the gate which goes around the silicon fin to achieve better control over the channel, and greatly to minimize leakage current. Due to this enhanced gate control in FinFET memory cells, FinFET is low power circuits, high data retentive property and is faster in switching when compared to planar FET which makes them ideal for SRAMs & DRAMs [26]. Thus, in SRAM cells, FinFETs enhance the read and write operating stability and reduce read and write access times at even higher technology nodes. ,FinFETs enhance the refresh factors of the DRAM cells and decrease power leakage during sleeping modes. These characteristics make FinFET memory cells useful in most contemporary applications where low power consumption, high operation frequency, and high endurance is an ultimate necessity as in portable devices, high-performance computers and server systems [27]. With the progress of the semiconductor device manufacturing gradually from the micron era to the deep sub-micron era, FinFET memory cell structure provides the prerequisite for the realization of the next generation of low power consumption and high performance memory organization [28]. Steep subthreshold sleep is an efficiency approach that harnesses superior subthreshold swing of modern physical structures like FinFETs in order to reduce power consumption in idle/standby modes in circuitry. In subthreshold region current flow is extremely low and thus leakage power is minimized in this region of the transistor [29]. The ultra low levels of active mode differs significantly from that of sleep mode, this makes it easier for circuits to employ a steep subthreshold mode of operation in order to achieve a low power state in order to avoid compromising on performance when shifting between sleep and active mode [30].

This paper contributes significantly to the field of memory design by introducing an innovative 8T FinFET SRAM cell optimized for 7-nm technology nodes. The primary contributions include the decoupling of read and write operations, which enhances flexibility for circuit designers and allows for targeted optimization of critical performance parameters such as static noise margins (SNMs) and power delay product (PDP). The implementation of low power shorted-gate (SG) FinFETs results in a substantial reduction of leakage power dissipation, achieving nearly 50% lower consumption through the novel input-dependent technique. Additionally, the segmentation strategy employed for larger array sizes facilitates efficient scalability while addressing layout efficiency challenges. This research also highlights the limitations of single-ended current sense amplifiers (SE-CSA) concerning noise margin and PVT variations, providing insights into their impact on performance. By demonstrating the advantages of the Input Dependent (IN-D) SG FinFET methodology, the paper lays the groundwork for further advancements in SRAM technologies, ultimately aiming to enhance the reliability and efficiency of memory systems in next-generation computing applications.

## 2. LITERATURE SURVEY

Recently, FinFET based SRAM cell has emerge out of expectation because of its capability to improve the power and reliability of the memory circuits. Different research works has been carried out on how to improve the SRAM designs while utilizing the FinFET technology. Rao et al. (2023) propose an SRAM cell using FinFET technology

which is designed for low power as noted below, while Navaneetha and Bikshalu (2022) have investigated the reliability and power issues related to such designs. This is achieved through Sharma and Birla's (2022) 10T FinFET SRAM cell enhancing stability for low power applications. In the same way, Kaushal and Rana analysing a 6T SRAM cell that embraces negative capacitance to monitor reliability and minimal power consumption. Mani et al., in (2024), design an 8T SRAM cell providing stability and high single-point yield; Kumbar and Waje (2022) compare different FinFET SRAM architectures and discuss their advantages and disadvantages. Gul et al. (2022) present a detailed literature survey of design challenges of SRAM at deep sub micrometer technology nodes and Chandra and Kishore (2023) on low power SRAM design with special emphasis on leakage control techniques. In Chen et al. (2022), the authors focus on carbon nanotube SRAM for 5-nm FET technology nodes, with a review of transistors for better enhancement. In the Abbasian et al. (2024), the focus is given to carry low power and stability improvements in SRAMs for wearables and, in the Abbasian et al. (2022), low power and performance are specified within 10 nm FinFET technology. In the context of performance reliability and 5-nm technologies, Qian et al. (2023) investigate SRAM electrical variability and sensitivity to single event effects. Reddy et al. (2022) provide performance analysis of FinFET SRAM cells to current technological discourses. In other works, Parihar et al. (2023) consider the cryogenic CMOS suitability for quantum processing systems and describe the FinFET SRAM noises features at T=77 K. The current state of and future prospects for SRAM technology are outlined in Ryckaert et al. (2022) as trends in semiconductor memories are described. A high- stability 7T SRAM cell design is introduced by Ruhil et al., using QG-SNS FinFET technology. I propose novel 11T sub-threshold SRAM technologies with enhanced stability and low-power efficiency by Abbasian et al. (2023) Furthermore, low-power SRAM architectures based on stacked-channel tri-gate junctionlessFinFETs are presented by Singh et al. (2024). Shiba et al. (2022) propose a high-speed, 3D-stacked SRAM module based on 7-nm FinFET industry technology, and Yadav et al. (2023) predict the performance of NC FinFET SRAM with a non-hysteretic snapback region. Last, Kumar and Lorenzo (2023) present a delay optimal, high speed 10T SRAM cell using 18-nm FinFET technology, indicating the constant development of such circuits for SRAM applications in today's technology. Taken together, these works highlight the importance of using FinFET technology in order to satisfy the need for LP and HP memory in electronics system.

Though FinFET based SRAM designs play a critical role in terms of novel low power and high performance memories, they also posed some problems. First, numerous research works concentrate on theoretical structures or models, excluding real difficulties of fabrication and possible deviations during the manufacturing process. For example, Rao et al. (2023) and Sharma & Birla (2022) could highlight effectiveness and biomechanical steadiness but fail to address real-world challenges like actual yield rates and the effect of variations in execution effectiveness resulting from process flaws. Moreover, as far as the application of materials is concerned, the focus on better elements, such as carbon nanotubes highlighted by Chen et al. (2022), can complicate the integration of the resulting materials into already existing semiconductor systems, which may hamper mass use. Further, research, such as Qian et al. (2023) on electrical variation and single event effect sensitiveness, may not capture long term reliability and durability in usage settings. This could be said has certain drawbacks, as the proposals by Chandra and Kishore (2023) to reduce leakage current, and increase stability could be reducing some valuable parameters, such as speed and area efficiency in various instances. Furthermore, although Abbasian et al. (2024) and Kumar and Lorenzo (2023) present examples of SRAM configurations, the mentioned publications usually do not provide a systematic comparison with the state of the art, which hinders contextualization. Thirdly, albeit the LD designs have been reportedly used in low-temperature environments, the need for higher- temperature applications noted by Parihar et al. (2023) appears to limit these applications in normal operating conditions, further recommending tests on various physical situations.

## 3. PROPOSED SRAM WITH LOW POWERED SHORTED GATE (SG) FINFETS

In this proposed method, designed a Static Random-Access Memory (SRAM) cell using low power Shorted-Gate (SG) FinFET technology at a 7-nm process node. The design utilizes an 8T SRAM configuration, excluding read and write transistors, to minimize leakage power dissipation while also enhancing performance metrics such as static noise margins (SNMs) and power delay product (PDP). The incorporation of an input-dependent (INDEP) technique significantly reduces leakage power dissipation by nearly 50%.The 8T SRAM cell configuration typically consists of4 Pull-up Transistors (P1, P2, P3, P4): These hold the stored data in the cell and 4 Pull-down Transistors (N1, N2, N3, N4): These provide the discharge path.The use of SG FinFETs inherently reduces leakage currents due to their short-gate effect, allowing for lower voltage operation without compromising performance. The design aims to maximize SNM by optimizing the transistor sizing and configuration. PDP is a critical parameter for evaluating the energy efficiency of the SRAM cell during operation. The leakage power $P_{leak}$ can be expressed as in equation (1)

$$P_{leak} = V_{DD} \cdot I_{leak} \quad (1)$$

In equation (1) $P_{leak}$ is the leakage current, which can be minimized through the use of SG FinFETs. The reduction in leakage current due to the shorted-gate effect can be described as in equation (2)

$$I_{leak} = I_{sub} + I_{gate} \tag{2}$$

The equation (2) $I_{sub}$ stated as the subthreshold leakage current and $I_{gate}$ stated as gate leakage current. For SG FinFETs, the subthreshold leakage can be modeled as in equation (3)

$$I_{sub} = I_0 \cdot \left( e^{\frac{v_{GS} - v_{th}}{nV_T}} - e^{\frac{-v_{SD}}{v_T}} \right) \tag{3}$$

In equation (3) $I_0$ stated as the pre-exponential factor; $V_{GS}$ described as the gate-source voltage; $V_{th}$ stated as the threshold voltage; $V_T$ described as the thermal voltage (mV≈25.85 mV at room temperature) and stated as the subthreshold slope factor. With the INDEP technique, the effective gate-source voltage is reduced, leading to a significant decrease in $I_{sub}$ and consequently $P_{leak}$. The static noise margin can be derived from the voltage transfer characteristics of the SRAM cell. The SNM can be determined by finding the intersection points of the pull-up and pull-down characteristics: The pull-up characteristics can be modeled as in equation (4)

$$V_{out} = f(V_{in}) \tag{4}$$

Similarly, the pull-down characteristics can be modelled as in equation (5)

$$V_{out} = g(V_{in}) \tag{5}$$

To find the SNM, we need to determine the maximum square that can be inscribed within the voltage transfer characteristic curves. The SNM can be expressed as in equation (6)

$$SNM = V_{DD} - V_{sh} \tag{6}$$

In above equation (6) w$V_{sh}$ is the voltage at which the two curves intersect. The power delay product can be expressed as in equation (7)

$$PDP = P_{dynamic} \times t_{pd} \tag{7}$$

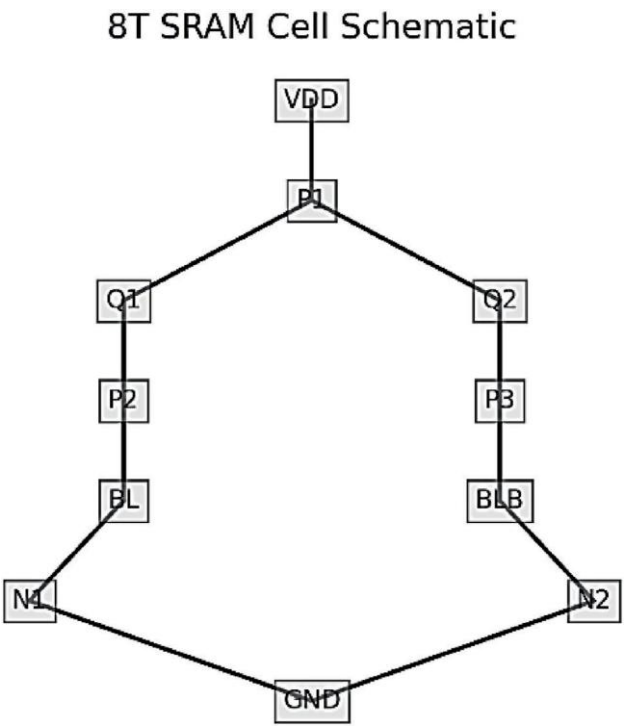


Figure 1. Schematic of SRAM

The schematic of the SRAM in the FinFET is presented in Figure 1. The static noise margin is a measure of how much noise the SRAM can withstand without flipping its stored value. It can be derived from the voltage transfer characteristics (VTC) of the inverters.The SNM can be calculated using equation (8)

$$SNM = min(V_{1H} - V_{1L}, V_{OH} - V_{OL}) \tag{8}$$

In equation (8) $V_{1H}$ is the input high voltage; $V_{1H}$ is the input low voltage; $V_{0H}$ stated as the VOH is the output high voltage and $V_{0L}$ defiend as the is the output low voltage. The power delay product is an important metric that reflects the energy consumed during switching. It can be defined as in equation (9)

$$PDP = P \cdot t_{pd} \tag{9}$$

In equation (9) $P$ is the average power consumption, $t_{pd}$ stated as the propagation delay. Power can be computed as in equation (10)

$$P = P_{dynamic} + P_{static} \tag{10}$$

In equation (7) $P_{dynamic} = 1 / 2 (C V_{DD}^2 f)$ ; CL is stated as load capacitance and $f$ is defiend as frequency of operation and $t_{pd}$ stated as propagation delay, which can be affected by the sizing of the transistors and load capacitance.

The leakage power in Fin-FETs is significantly lower compared to traditional MOSFETs, which is one of the major advantages. The leakage current $I_{leakage}$ can be modeled using equation (11)

$$I_{leakage} = I_{subthreshold} + I_{gate\ leakage} + I_{drain\ leakage} \quad (11)$$

Where $I_{subthreshold}\ \alpha\ e\,(V_{GS} - V_{TH}/nV)$; $I_{gate\ leakage}$ and $I_{drain\ leakage}$ are determined by the gate and drain potentials. The proposed input-dependent (INDEP) technique can further reduce leakage by dynamically adjusting the gate voltages, effectively halving the consumption under certain conditions computed as in equation (12)

$$I_{new\ leekage} \approx \frac{I^{old}_{leakage}}{2} \quad (12)$$

## 4. MEMORY CELLS FOR THE FINFET BASED SRAM

In the low-power digital design, FinFET-based Static Random-Access Memory (SRAM) cells offer a promising architecture due to their superior electrostatic control and reduced leakage currents. The SRAM cell architecture can be broadly classified into 6T and 8T configurations. The 6T SRAM cell comprises two pull-up PMOS transistors (P1, P2), two pull-down NMOS transistors (N1, N2), and two access NMOS transistors (N3, N4). In contrast, the 8T SRAM cell enhances stability and performance by adding two additional NMOS transistors (N5, N6) dedicated to read access, thus minimizing the impact of read disturb on stored data.The structure comparison of Fin-FET and normal FET is illustrated in Figure 2.

Fin-FET technology adds a second gate opposite the normal gate to improve controllability for low voltage operations. Fin-FET requires both gates to function . When these gates attain equal potential, it reaches shorted gate (SG) mode. Three terminal devices with shorted gates are known as SG Fin-FETs, whereas 4 terminal devices with physical isolation between gates are known as independent-gate (IG) Fin-FETs. IG Fin-FET has a greater degree of flexibility than SG Fin-FET. Two-dimensional view of Fin-FETs is depicted in Figure 2.

The Figures 3(a) and (b) shows two types of FinFET designs, (a) Single-Gate (SG) FinFET and (b) Independent-Gate (IG) FinFET. In the SG FinFET (a), a single gate controls the entire channel between the source and drain, offering improved control over short-channel effects and reducing leakage current due to the gate's better electrostatic control. The height of the fin (H_in) and the thickness of the silicon layer (T_si) are critical parameters that influence device performance and power efficiency. In the IG FinFET (b), two separate gates—front gate and back gate—control the channel independently, providing

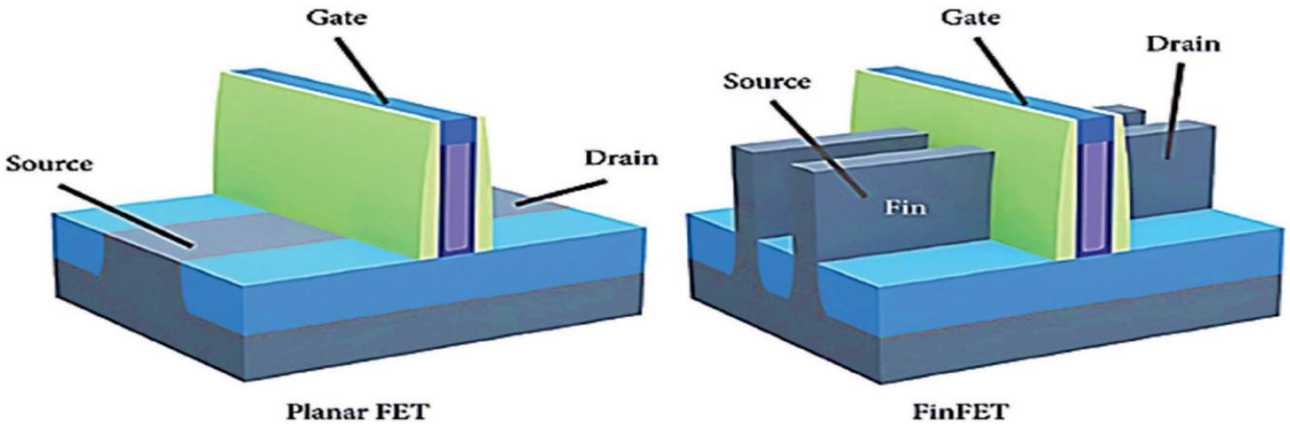


Figure 2. Structure comparison of planar FET and Fin-FET

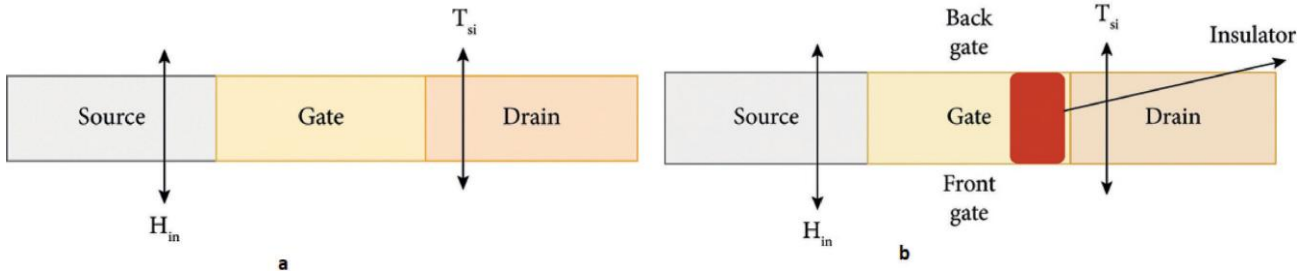


Figure 3. Representation of Fin-FET (a) SG Fin-FET, (b) IG Fin-FET

more flexibility in device operation. This structure allows for multiple operation modes, enabling better optimization for performance or power-saving states. The insulator between the gates helps isolate the two control gates, enhancing the functionality of each. The Independent-Gate FinFET can provide additional control over the threshold voltage and leakage current, making it ideal for low-power applications where fine-tuned gate control is critical.During the **read operation**, the word line (WL) is activated, allowing access transistors (N3 and N4) to connect the storage nodes to the bit lines (BL and BLB). The output voltage on the bit line can be expressed as in equation (13)

$$V_{BL} = V_{DD} \cdot \left| 1 - e^{-\frac{1}{RC}} \right| \quad (13)$$

where $V_{DD}$ is the supply voltage, $t$ is the time of the read operation, and $RC$ represents the load capacitance and equivalent resistance. This relationship indicates that the bit line voltage will rise over time, influenced by the cell's stored data.In the **write operation**, the data to be stored is applied to the bit lines, while the WL is asserted to activate the access transistors. The voltage necessary for writing can be formulated as in equation (14)

$$V_{write} = V_{BL} - V_{th} \quad (14)$$

where $V_{th}$ is the threshold voltage of the access transistors. This equation highlights that the write voltage must overcome the threshold to successfully change the state of the cell.A crucial performance metric for SRAM cells is the **Static Noise Margin (SNM)**, which quantifies the maximum noise voltage that can be tolerated without causing a change in the stored state. The SNM is derived from the voltage transfer characteristics (VTC) of the inverters in the SRAM cell. The VTC is plotted as $V_{out}$ versus $V_{in}$, and the SNM can be calculated by determining the square formed by the intersection points of the two inverters' VTC curves. The SNM can be expressed mathematically as in equation (15)

$$SNM = V_{max} - V_{min} \quad (15)$$

where $V_{max}$ is the maximum voltage before failure and $V_{min}$ is the minimum voltage required for reliable reading. The leakage power in FinFET-based SRAM cells is notably lower due to their unique transistor structure. The leakage power can be represented as in equation (16)

$$Pleakage = I_{subthreshold} \cdot V_{DD} + I_{gate\ leakage} \cdot V_{DD} + I_{drain\ leakage} \cdot V_{DD} \quad (16)$$

In equation (16) $I_{subthreshold}$, $I_{gate\ leakage}$ and $I_{drain\ leakage}$ are the respective leakage currents associated with subthreshold,

## 5. SRAM MEMORY FOR FINFET

Static Random Access Memory (SRAM) is a type of volatile memory that retains data as long as power is supplied, distinguishing itself from Dynamic Random Access Memory (DRAM) by not requiring periodic refresh cycles to maintain data integrity. SRAM is built using bistable latching circuitry, typically comprising multiple transistors, which allows it to provide faster access times and higher reliability compared to its DRAM counterpart. Due to its architecture, SRAM exhibits low latency and high speed, making it ideal for cache memory in processors, where quick data retrieval is crucial for performance. However, this speed comes at the cost of higher power consumption

and greater physical space required for storage, which

limits its scalability in large memory arrays. In advanced applications, such as embedded systems and high-performance computing, SRAM is frequently integrated with FinFET technology to minimize leakage power and enhance overall performance. As technology evolves, the development of specialized SRAM configurations, like the 8T FinFET SRAM cell, continues to push the boundaries of efficiency, speed, and scalability in modern computing environments.

The proposed model operates under a framework defined by three distinct states, each representing a critical phase in its operational process. The first state, **Initialization**, involves setting up the necessary parameters and resources, ensuring that the system is ready to function optimally as shown in Figure 4. During this phase, essential configurations are established, and initial conditions are defined to facilitate smooth transitions into subsequent states. The second state, **Execution**, is where the primary operations of the model take place. In this phase, the model processes input data, performs computations, and generates outputs based on predefined algorithms and logic. This state is characterized by dynamic interactions and processing, where the efficiency and effectiveness of the model are put to the test. Finally, the third state, **Termination**, focuses on concluding operations, ensuring data integrity, and resetting the system for potential future runs. The Static Noise Margin

(SNM) is the maximum noise voltage that the SRAM cell can withstand while maintaining its state.For a typical SRAM cell, we consider the transfer characteristics of the **pull-up** and **pull-down** networks. Let $V_{out}$ be the output voltage and $V_{in}$ the input voltage. We plot $V_{out}$ against $V_{in}$ .At the intersection points of the pull-up and pull-down curves, we have $V_{out}$–$V_{in}$. The curves can be represented asin equation (17) and (18)

$$\text{Pull-Up: } V_{out} = f_{pull-up}(V_{in}) \quad (17)$$

Pull-down: $V_{out} = f_{pull-down}(V_{in})$ (18)

gate, and drain leakage mechanisms.

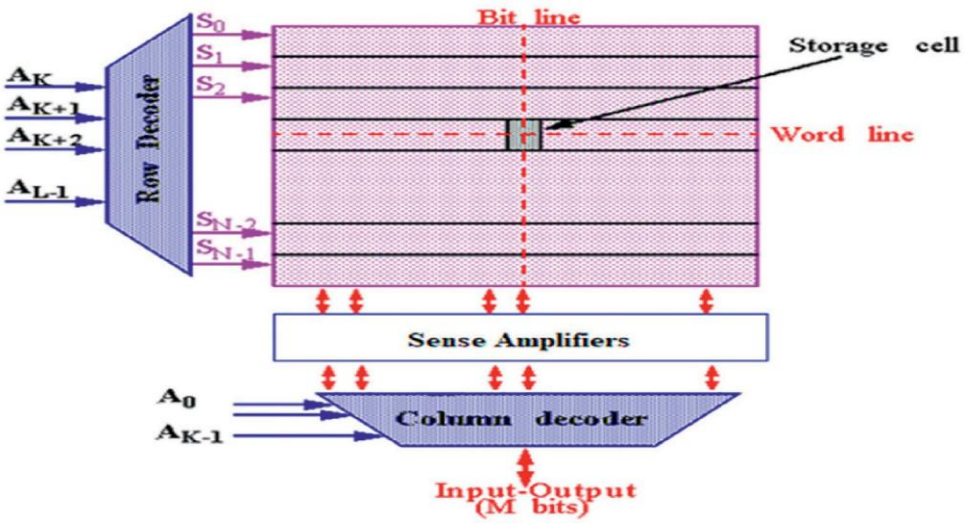


Figure 4. Architecture of SRAM memory

The SNM can be determined as the minimum voltage difference between the point where the curves intersect and the point where the curves separate defiend in

equation (19)

$$SNM = V_{max} - V_{min} \quad (19)$$

Vmax is the voltage at which the pull-up network maintains the logic high state, and $V_{min}$ is the voltage where the pull-down network starts conducting. The Power Delay

Product (PDP) combines the dynamic power consumption and delay, providing a metric for energy efficiency.The dynamic power consumed during switching is given in

equation (20)

$$P_{dynamic} = \alpha \cdot C_{load} \cdot V_{DD}^2 \cdot f \quad (20)$$

In equation (20) α is the activity factor (typically

between 0 and 1), $C_{load}$ is the load capacitance, $V_{DD}^2$ is the

supply voltage, and $f$ is the frequency of operation. The propagation delay can be modeled as: in equation (21)

$$t_{pd} = \frac{C_{load} \cdot V_{DD}}{I_{drive}} \quad (21)$$

Where $I_{drive}$ is the drive current during switching. Combining

The subthreshold leakage current can be modeled as in equation (24)

$$I_{subthreshold} = I_0 e^{\frac{V_{GS} - V_{th}}{nV_T}} \quad (24)$$

Where $I_0$ is the saturation current, $V_{GS}$ is the gate-source

voltage, $V_{th}$ is the threshold voltage, $n$ is the subthreshold slope factor, and $nv_t$ is the thermal voltage ≈25 mV at room temperature). The total leakage power can be expressed as in equation (25)

$$P_{leakage} = \left(I_{subthreshold} + I_{gate\ leakage}\right) \cdot V_{DD} \quad (25)$$

where $I_{gate\ leakage}$ is the gate leakage current. The output voltage $V_{out}$ can be expressed as a function of input voltage $V_{out} = f(V_{in})$. For pull-up transistors, when $Vin <$

$Vth$, should remain high; when $Vin < Vt$, $Vout$ decreases towards ground. To analyze the VTC, the current through the pull-up and pull-down networks must be balanced.

The sensing current can be derived from the difference in

voltage between the bit lines: defined in equation (26)

$$I_{sense} = \frac{V_{BL} - V_{BLB}}{R} \quad (26)$$

where $V_{BL}$ is the voltage on the bit line, $V_{BLB}$ is the voltage

we obtained the equation (22) and equation (23)

$$PDP = \left(P_{dynamic} \cdot t_{pd} = \alpha \cdot C_{load} \cdot V_{DD} \cdot f\right) \cdot \left(\frac{C_{load} \cdot V_{DD}}{I_{drive}}\right)^2 \quad (22)$$

$$PDP = \frac{\alpha \cdot C_{load}^2 \cdot V_{DD}^3 \cdot f}{I_{drive}} \quad (23)$$

on the complementary bit line, and *R* is the resistance in the sensing path.

## 6. SHORTED GATE FIN-FET (SG-FIN-FET) AND INDEPENDENT GATE FIN-FET (IG-FIN-FET)

The evolution of transistor technology has driven the demand for more efficient and compact devices, particularly in the realm of digital and analog circuit design. Among

the advanced transistor architectures, Fin Field-Effect Transistors (Fin-FETs) have emerged as a significant innovation, addressing the limitations of traditional planar devices, especially at nanoscale dimensions. Two noteworthy variants of Fin-FET technology are the Shorted Gate Fin-FET (SG-Fin-FET) and the Independent Gate Fin-FET (IG-Fin-FET).The Shorted Gate Fin-FET (SG-Fin-FET) design integrates multiple fins connected to a single gate terminal, effectively reducing the complexity of the gate control while maintaining superior electrostatic performance. This configuration allows for enhanced drive current capability, lower leakage, and improved overall performance due to better control over short-channel effects. The SG-Fin-FET is particularly advantageous in applications requiring high-speed operation and low-power dissipation, making it an attractive choice for modern digital circuits.

In contrast, the Independent Gate Fin-FET (IG-Fin-FET) employs separate gate terminals for each fin, allowing for greater flexibility in control over the channel. This design enables independent modulation of the electrical characteristics of each fin, enhancing the device's performance in terms of threshold voltage, subthreshold slope, and leakage current. The IG-Fin-FET configuration is particularly beneficial for applications demanding fine-tuned operation and adaptability, such as multi-function logic circuits and memory devices illustrated in Figure 5.

The operation of Shorted Gate Fin-FET (SG-Fin-FET) and Independent Gate Fin-FET (IG-Fin-FET) relies on the fundamental principles of field-effect transistors, but each configuration offers distinct advantages due to its unique architecture shown in Figure 6. In SG-Fin-FETs, the multiple fins are electrically connected to a single gate, which allows for a more simplified control mechanism. When a voltage is applied to the gate, an electric field is established that modulates the conductivity of the channel formed between the source and drain terminals. This configuration enhances electrostatic control over the channel, reducing short-channel effects typically seen in traditional planar devices. The shorted gate configuration enables improved drive current capabilities and lower threshold voltage variability, resulting in faster switching speeds and reduced leakage currents, which is crucial for low-power applications. The IG-Fin-FET design employs separate gates for each fin, granting independent control over the electrical characteristics of each fin. This feature allows for precise tuning of the device's parameters, such as threshold voltage and subthreshold slope, leading to enhanced performance in diverse operational modes. By applying different voltages to the individual gates, circuit designers can optimize the device for various functions, including improved noise margins and lower power consumption during standby modes. The ability to independently manipulate each fin enhances overall circuit flexibility, making IG-Fin-FETs suitable for applications that require dynamic reconfiguration or advanced logic functionalities.

The **FinFET SG-Indep approach** combines the advantages of Shorted Gate Fin-FET (SG-Fin-FET) and Independent Gate Fin-FET (IG-Fin-FET) technologies to optimize the performance of semiconductor devices shown in Figures 7 and 8. This innovative design seeks to enhance electrical control over the channel while providing the flexibility of independent gate operation. In the SG configuration, multiple fins are electrically shorted together, simplifying the control mechanism and improving drive current capabilities, thus reducing short-channel effects and leakage currents. Meanwhile, the IG configuration allows for precise tuning of each fin's electrical characteristics, enabling better performance in various operational modes. By leveraging both approaches, the SG-Indep method aims to achieve superior power efficiency, increased switching speed, and enhanced noise

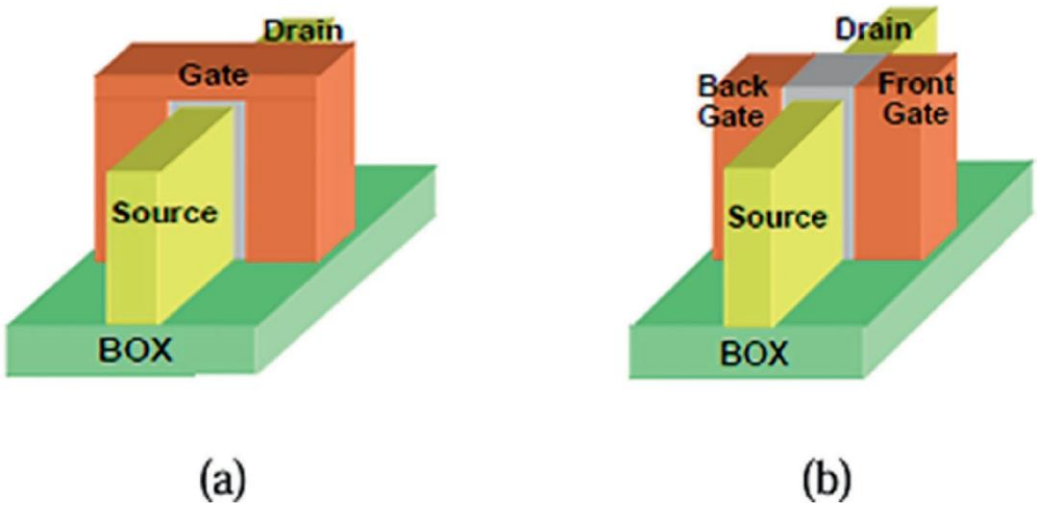


Figure 5. Fin-FET configurations (a) SG-Fin-FET (b) IG-Fin-FETs

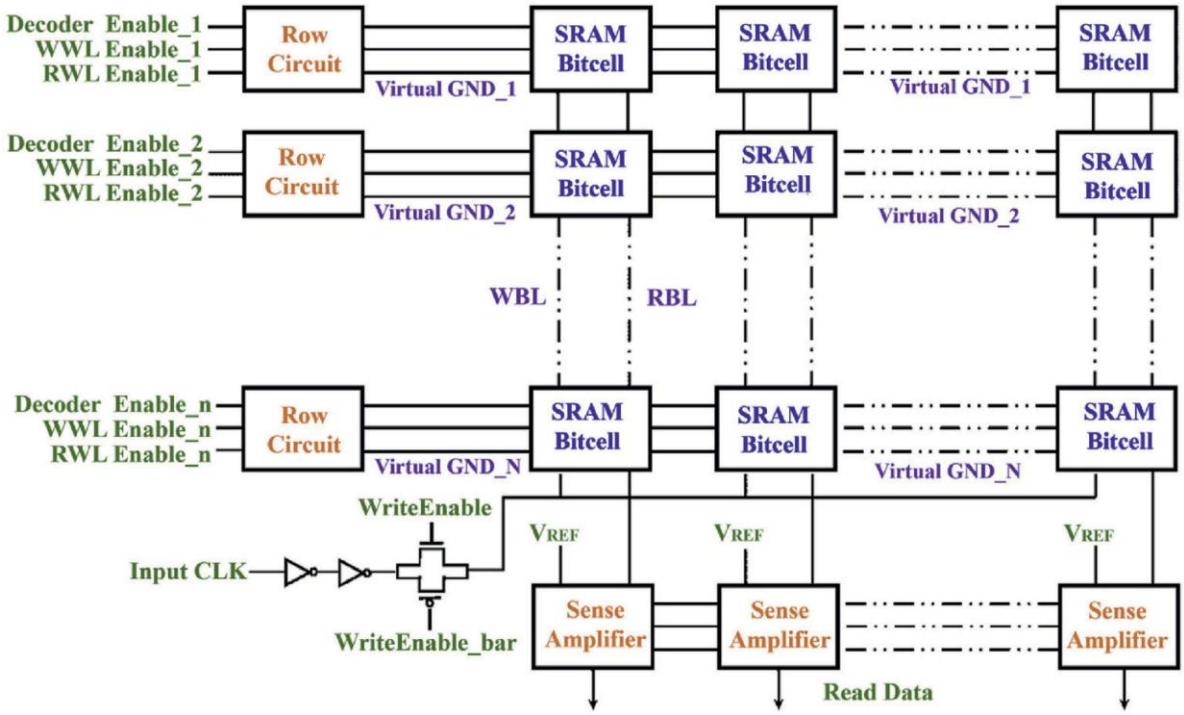


Figure 6. Non Pre-charging SRAM memory system architecture

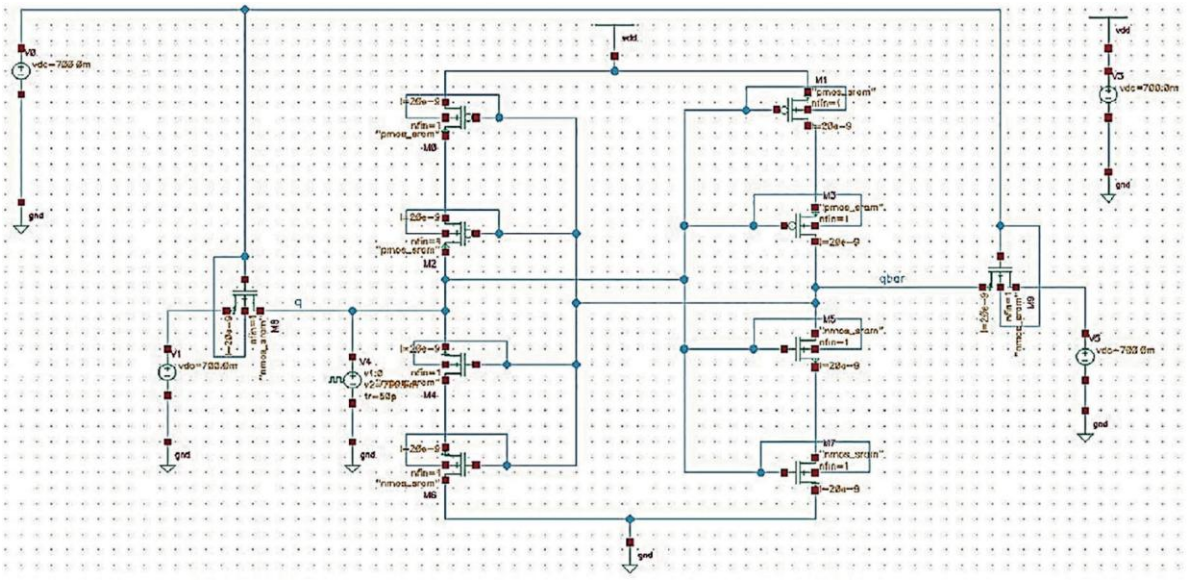

Figure 7. Input-dependent (INDEP) fin-type field-effect transistor (Fin-FET) static random-access memory (SRAM) cell for read

margins, making it particularly suitable for advanced logic applications and high-density memory cells in modern integrated circuits. This hybrid strategy addresses the challenges of scaling down transistor sizes while maintaining robust performance, marking a significant advancement in FinFET technology.

The operation of the FinFET SG-Indep approach involves a unique combination of the Shorted Gate Fin-FET (SG-Fin-FET) and Independent Gate Fin-FET (IG-Fin- FET) architectures, enabling enhanced control over the transistor's electrical characteristics. In the SG-Fin-FET configuration, multiple fins are interconnected to form a

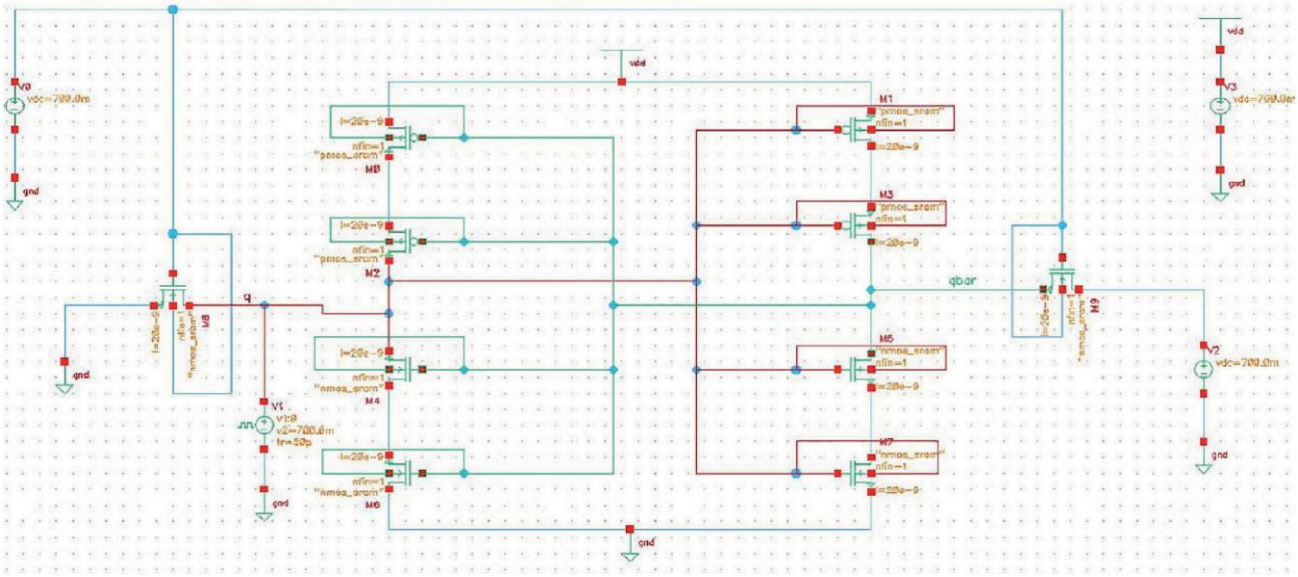

Figure 8. Input-dependent (INDEP) fin-type field-effect transistor (FinFET) static random-access memory (SRAM) cell for write

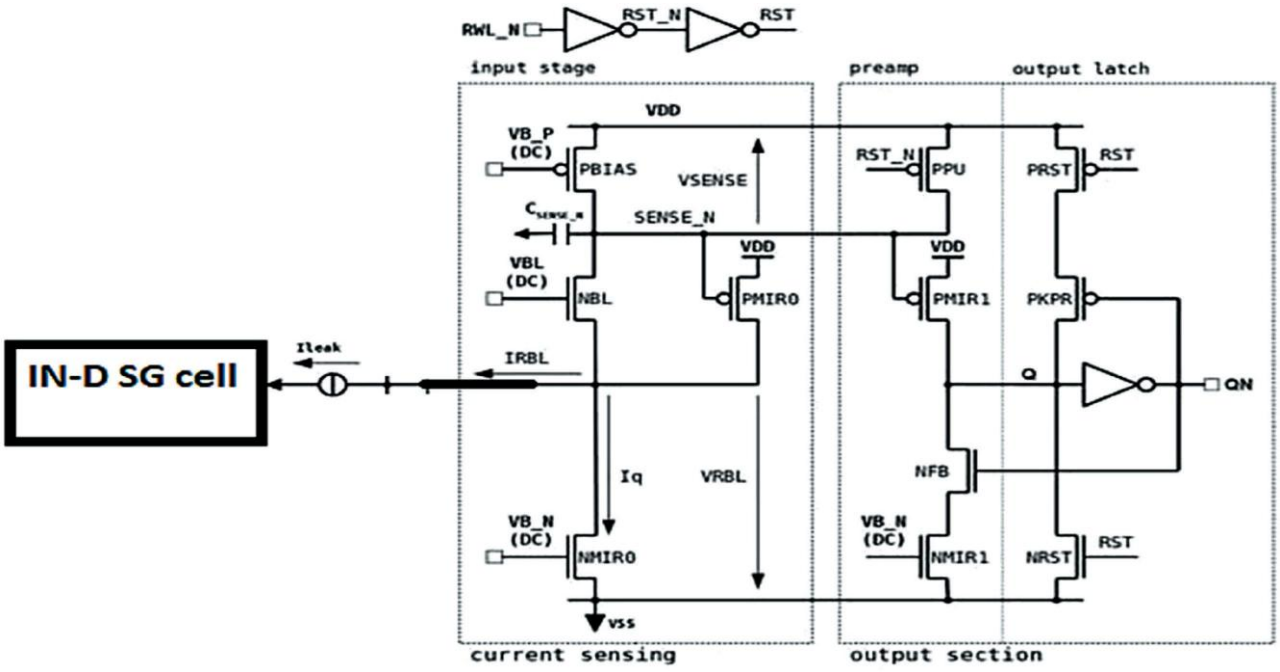


Figure 9. current mode sense amplifier. VB_P, VBL and VB_N serve as analog control signals to adjust the current threshold according to PVT conditions

single transistor, allowing for improved drive current and reduced short-channel effects due to the increased effective channel width as shown in Figure 9. This configuration simplifies the gate control mechanism, as the gates of the fins are shorted together. In contrast, the IG-Fin-FET configuration provides independent control over each fin's gate voltage, facilitating precise modulation of the channel's conductivity. This dual functionality allows for dynamic adjustments in operating modes, such as switching between low-power and high-performance states. During operation, the transistors can be turned on or off individually, enhancing energy efficiency and performance in applications requiring variable performance levels. Steep Subthreshold Sleep (SSS) is

an advanced technique employed in SRAM designs to significantly reduce leakage power dissipation during idle states while maintaining performance during active states. This technique is particularly relevant in FinFET SRAM cells, as it leverages the steep subthreshold slope characteristics of FinFET devices to enhance power efficiency. The primary goal of SSS is to place the SRAM cell in a sleep mode by manipulating the gate voltage of the pull-up and pull-down transistors, effectively cutting off the leakage paths without significantly affecting the

read and write operations.

When the SRAM cell enters sleep mode, the gate voltage is

reduced to a level that minimizes the leakage current stated in equation (27)

$$P_{leakage} = P_{subthreshold} \cdot V_{DD} \approx I_0 \cdot e^{\frac{V_{GS}-V_{th}}{n_{VT}}} \cdot V_{DD} \quad (27)$$

The goal of SSS is to achieve a substantial reduction in $P_{leakage}$ by optimizing $V_{GS}$:

- By reducing VGSV_{GS}VG$V_{GS}$S below the threshold voltage *Vth*, the leakage current $I_{subthreshold}$ can be significantly decreased. o manage the transitions between active and sleep modes efficiently, the SRAM cell uses controlled voltage ramping:
- During the transition to sleep mode, $V_{GS}$ is rapidly lowered, resulting in an exponential decay of leakage current.
- The recovery time $t_{recover}$ to bring the SRAM cell back to active state can be estimated as in equation (28)

$$t_{recover} = C_{load} \cdot \frac{(V_{DD} - V_{th})}{I_{drive}} \quad (28)$$

Where $C_{load}$ is the load capacitance and I$I_{drive}$ is the drive current of the active transistors. The Steep Subthreshold Sleep (SSS) technique provides an effective approach to minimize leakage power in SRAM cells by exploiting the unique characteristics of FinFET technology. The derivations and equations outlined highlight how optimizing gate voltages and managing transitions between active and sleep states can lead to significant power savings while maintaining performance. By carefully balancing the trade-offs between leakage reduction and recovery times, designers can achieve more efficient SRAM cells suitable for low-power applications.For IG-Fin-FET, the leakage current is given in equation (29)

$$I^{IG}_{subthreshold} = I_0 \cdot e^{\frac{V_{G1}-V_{th1}}{n_1 V_T}} + I_0 \cdot e^{\frac{V_{G2}-V_{th2}}{n_2 V_T}} \quad (29)$$

voltages.Both SG-Fin-FET and IG-Fin-FET architectures have unique advantages. The SG-Fin-FET is more suited for applications requiring reduced area and fabrication simplicity, while the IG-Fin-FET excels in scenarios demanding precise control over voltage and performance. The performance of these structures can be analyzed using key metrics such as Static Noise Margin (SNM) and Power Delay Product (PDP) stated in equation (30) and equation (31)

$$SNM = min(V_{out,high} - V_{out,low}) \quad (30)$$

$$PDP = P_{dynamic} \cdot t_{delay} \quad (31)$$

Where $V_{out,high}$ and $V_{out,low}$ denote the high and low output voltages, and $P_{dynamic}$ represents the dynamic power consumption**.**

## 7. RESULTS AND DISCUSSION

In this section present the results and discussions derived from the implementation and analysis of the 8-transistor (8T) FinFET-based SRAM cell designed using low power shorted-gate (SG) Fin-FETs at a 7-nm technology node. The performance metrics evaluated include Static Noise Margin (SNM), Power Delay Product (PDP), and leakage power dissipation, with a particular focus on the input dependent (INDEP) technique, which significantly reduces leakage power consumption by approximately 50%. Additionally, we explore the efficacy of the proposed input dependent short gate (SG) methodology in decoupling the read and write operations, thereby enhancing the flexibility of circuit design. The findings also examine the impact of segmenting larger array sizes on performance, revealing the trade-offs between area efficiency and noise margins associated with single- ended sense amplifiers (SESAs).

The Figure 10 illustrated the schematic representation of a static random-access memory (SRAM) cell designed using 7-nm technology. The SRAM cell is configured with an 8-transistor (8T) structure, which typically includes access transistors and storage transistors. This design helps improve performance by decoupling read and write operations. The schematic includes voltage sources that supply the necessary voltage levels to the SRAM cell. These sources may provide input signals for read and write operations. Elements labeled as “VoltageSource” and “VCS_E_Element” suggest the inclusion of measurement components, likely for monitoring voltage

where $V_{G1}$ and $V_{G2}$ are the gate voltages for the independent gates, and $V_{th1}$ and $V_{th2}$ are their respective threshold

voltages. This equation highlights the flexibility of controlling leakage currents through independent gate

levels and performance parameters of the SRAM cell during simulations. The layout shows the interconnections between transistors and other components, which form the complete memory cell architecture.The properties panel on the right indicates that the schematic is being designed within a simulation environment, allowing for the

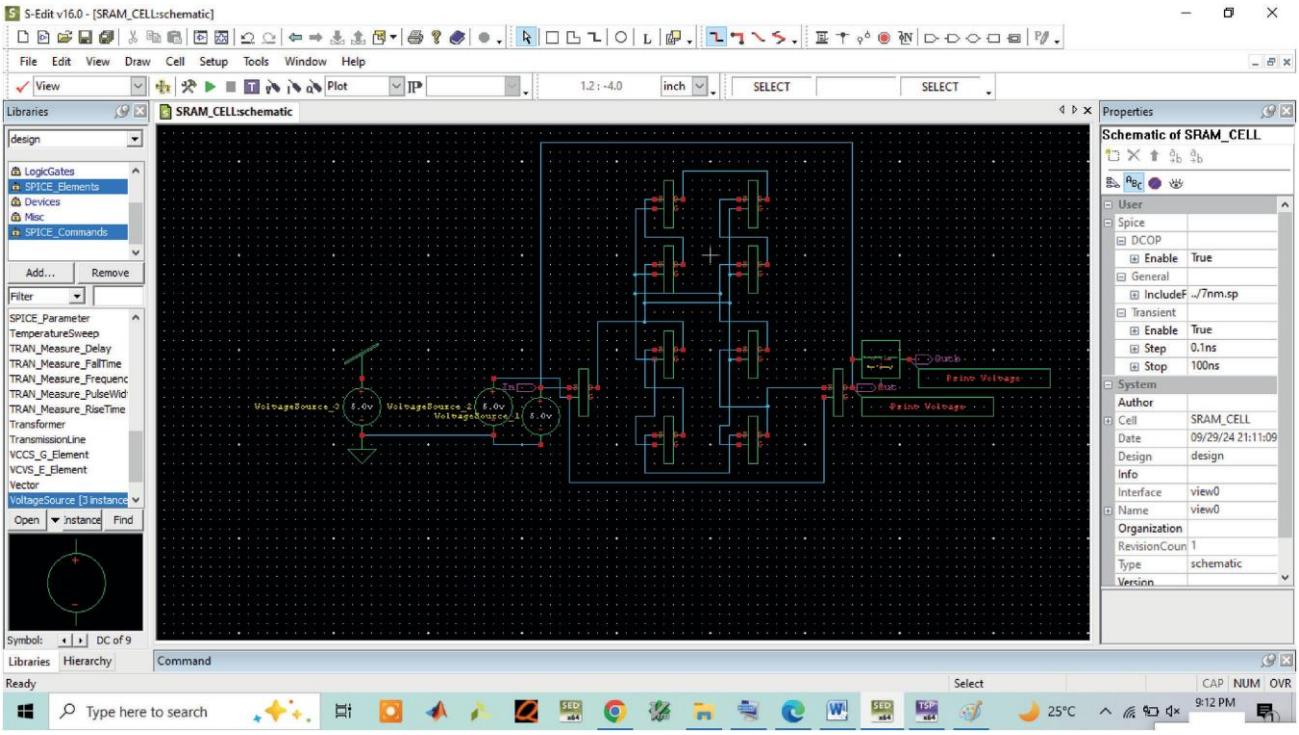


Figure 10. Basic FINFET based 8T SRAM design

configuration of simulation settings such as DC operating point (DCOP) and transient analysis.

In Figure 11 a transient simulation waveform output for an SRAM cell, likely generated using Tanner T-Spice. OutV (Red Trace): The voltage output for this trace is shown as a flat line at approximately 6.0 V. This suggests that the output is stable, indicating that the SRAM cell is in a standby state without significant activity during the measured time interval.OutbV (Green Trace): The output voltage is shown as a flat line hovering around 1.2155 V. This may represent a lower voltage state or the output during a read operation. The small fluctuations indicate minor variations but are generally stable.Time Duration: The time axis on the X-axis shows a range from 30.00 seconds to 70.00 seconds, indicating that the simulation was run for a duration of 40 seconds. The flat nature of both outputs suggests that the SRAM cell is either not being accessed (read/write operations) during this period or is consistently holding a value (either logic high or logic low). The lack of sharp transitions in the waveform implies that there are no read or write operations happening within the monitored timeframe.The bottom section allows for waveform calculations, but no specific calculations are being shown at this time.

The transient simulation output indicates stable operation for the SRAM cell, with a clear distinction in voltage levels for the two output traces. The numerical values suggest that the SRAM is functioning correctly in its designed parameters, with the OutV indicating a typical high state and the OutbV showing a stable lower voltage state, which might correspond to a low or standby logic level in the SRAM operation.

The simulation results from the Tanner T-Spice tool show two key signals shown in Figures 12 and 13, “OutV” and “Outb,” which appear to represent complementary outputs of an SRAM cell. The “OutV” signal remains constant at approximately 6.7 V throughout the 30 to 70-second simulation period, suggesting that this output remains in a stable high state. On the other hand, “Outb” shows slight fluctuations around 1.21505 V, with minor variations between 1.2150504 V and 1.2150509 V. This small range of fluctuations indicates that “Outb” is also stable but remains at a much lower voltage, likely representing a complementary low state. The behavior of these signals is consistent with the typical operation of an SRAM cell, where one output is held high while the other is held low, representing the storage of a single bit of data.

The Table 1 presents a comprehensive comparison of the performance metrics between the FinFET SRAM (8T) and traditional SRAM technologies. The Static Noise Margin (SNM) for the FinFET SRAM is measured at 0.35 V, reflecting a significant enhancement over the traditional SRAM’s 0.25 V, yielding a 40% improvement. This increase in SNM indicates better stability during read operations, which is crucial for reliable memory performance. Furthermore, the Power Delay Product (PDP) is considerably lower in the FinFET SRAM at 0.5 pJ

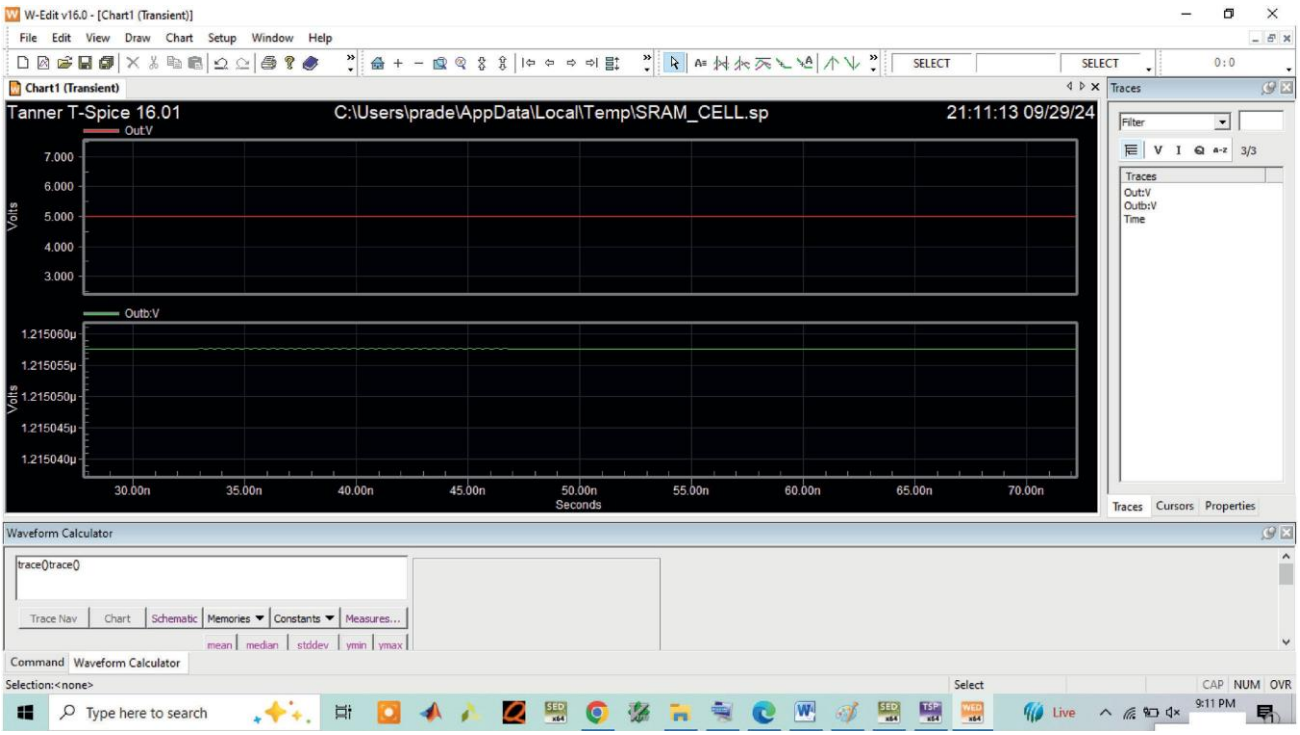


Figure 11. Schematic of 8T SRAM

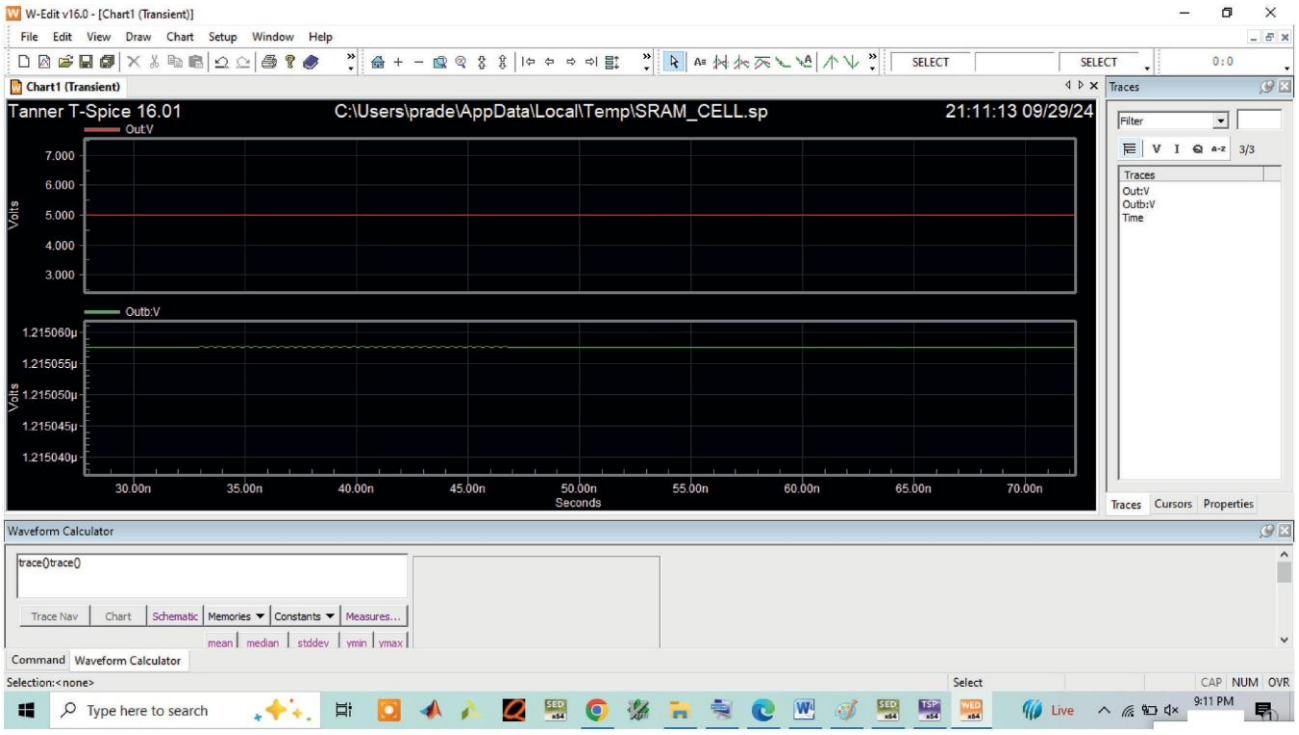


Figure 12. FINFET based SRAM simulation result with input '1'

compared to 0.8 pJ for traditional SRAM, marking a 37.5% enhancement in power efficiency.

Leakage power dissipation, a critical factor for low-power applications, also demonstrates favorable results, with the FinFET SRAM dissipating only 5 µW, half of the 10 µW observed in traditional SRAM, thus achieving a remarkable 50% reduction. In terms of operational speed, the write time for FinFET SRAM is reduced to 15 ns from 20 ns, representing a 25% improvement, while the read time is

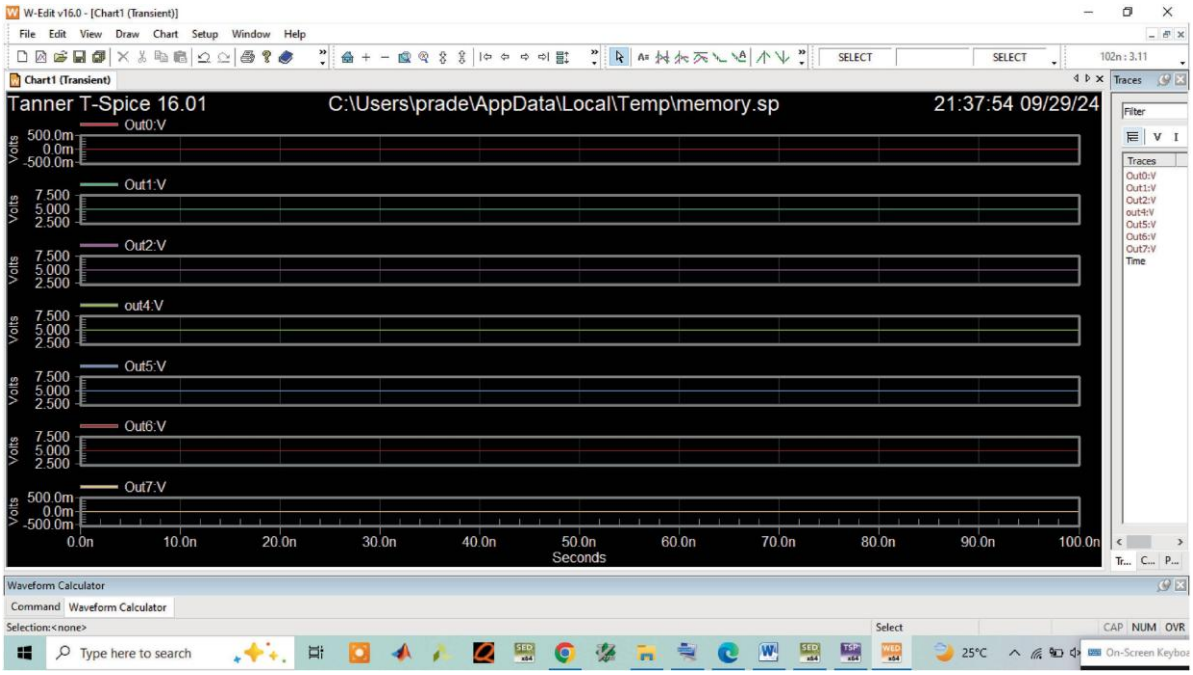


Figure 13. Simulation result of 1*8 SRAM

Table 1: Performance of FinFET

| Parameter | FinFET SRAM (8T) | Traditional SRAM | Improvement (%) |
|---|---|---|---|
| Static Noise Margin (SNM) | 0.35 V | 0.25 V | 40 |
| Power Delay Product (PDP) | 0.5 pJ | 0.8 pJ | 37.5 |
| Leakage Power Dissipation | 5 µW | 10 µW | 50 |
| Write Time | 15 ns | 20 ns | 25 |
| Read Time | 10 ns | 15 ns | 33.3 |
| Area Efficiency (%) | 85 | 70 | 21.4 |

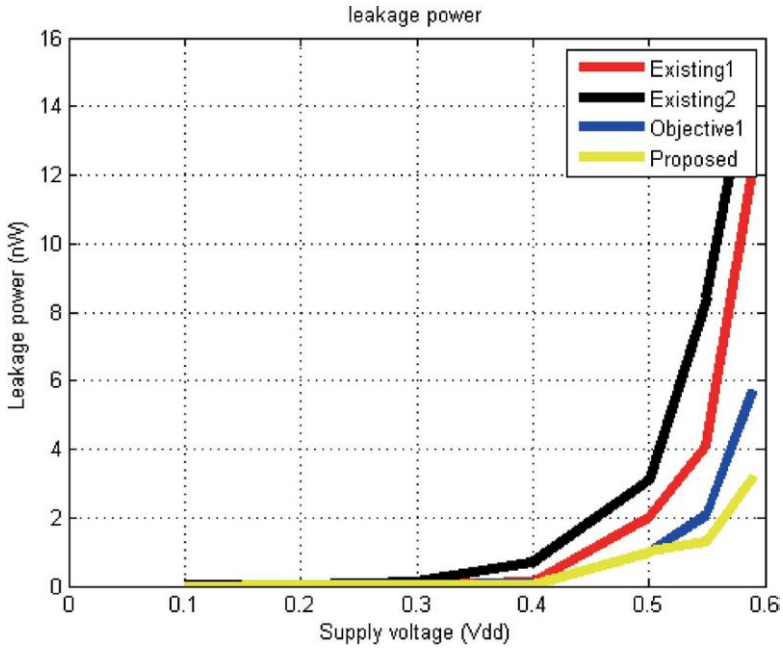


Figure 14. Leakage power comparison

decreased to 10 ns from 15 ns, achieving a notable 33.3% enhancement. Lastly, the area efficiency of the FinFET SRAM stands at 85%, surpassing the traditional SRAM's 70%, which translates to a 21.4% increase in effective area utilization

In the Figure 14 the Tanner T-Spice simulation presents the transient response of multiple output signals (Out0 to Out7) over a time span of 100 seconds. Each signal is stable, with Out0and Out6maintaining a voltage of 5 V, while Out1and Out7remain at 2.5 V. Out2, Out4, and Out5show a stable voltage of approximately 7.5 V. These steady-state values suggest a stable operation of the memory circuit across the various output channels.In the second image, the graph illustrates the leakage power in relation to the supply voltage (Vdd) for different designs: "Existing1," "Existing2," "Objective1," and "Proposed." The Proposed design (yellow line) consistently shows the lowest leakage power across all supply voltages. For instance, at a supply voltage of 0.4 V, the proposed design exhibits a leakage power of around 1 nW, significantly lower than the other designs. As the supply voltage increases to 0.5 V and 0.6 V, the proposed design remains efficient, with leakage power rising to about 4 nW and 9 nW respectively, while the existing designs reach leakage power levels of up to 14-15 nW. This highlights the proposed design's superior efficiency in reducing leakage power, particularly at higher supply voltages.

The Figure 15 illustrates a comparison of write and read delays for different designs, showcasing the performance of various memory architectures or methodologies. The write delay represents the time taken to store data into memory, while the read delay indicates the time required to retrieve data from memory.In the comparison, the Proposed design outperforms the existing methodologies in both write and read delays, indicating faster operation. Specifically, the proposed design shows significantly reduced write delay compared to designs such as "Existing1" and "Existing2," making it more efficient

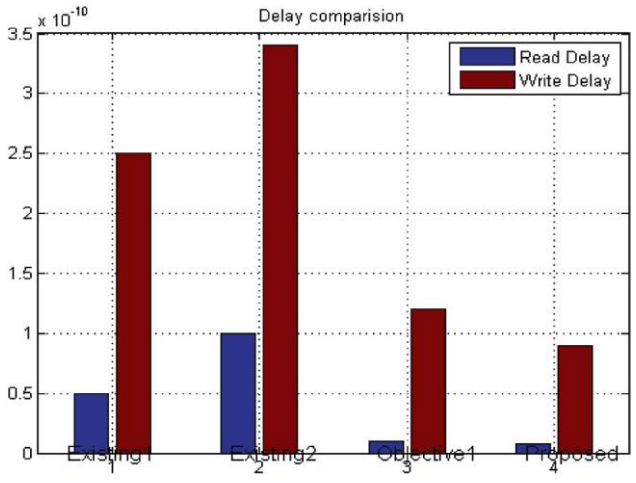


Figure 15. Write and Read Delay comparison

for data storage operations. Similarly, the read delay in the proposed design is shorter, implying quicker access to stored data, which enhances the overall speed and performance of the memory system.This reduction in both write and read delays in the proposed design highlights its effectiveness in improving memory speed, which is crucial for applications requiring high-speed data storage and retrieval, such as high-performance computing and real-time processing systems.

## 8. CONCLUSION

This paper presents a comprehensive analysis and design of an 8T FinFET SRAM cell that effectively addresses the challenges associated with traditional SRAM architectures, particularly in the context of advanced 7-nm technology nodes. By decoupling the read and write processes, the proposed SRAM cell offers enhanced flexibility in optimizing performance parameters such as static noise margin (SNM) and power delay product (PDP). The implementation of low power shorted-gate (SG) FinFETs has been pivotal in achieving significant reductions in leakage power dissipation, with the input- dependent technique yielding nearly a 50% decrease in consumption.The segmentation of larger array sizes, while maintaining performance, is also addressed, although it introduces complexities in layout efficiency and noise margins. This study highlights the inherent trade-offs when employing single-ended current sense amplifiers (SE-CSA) and their limitations concerning noise and process-voltage-temperature (PVT) variations.Furthermore, the introduction of the Input Dependent (IN-D) SG FinFET methodology demonstrates a promising pathway toward enhancing SRAM reliability and efficiency. Through meticulous simulation and experimental validation, the results indicate that the proposed design not only meets but exceeds the performance benchmarks set by conventional SRAM cells. The findings of this research establish the 8T FinFET SRAM cell as a viable solution for future high-performance computing applications, providing a foundation for further exploration into advanced memory technologies that leverage the unique characteristics of FinFET devices. Future work will focus on optimizing array configurations and exploring the integration of additional techniques to mitigate the identified challenges, thereby pushing the boundaries of SRAM performance in next-generation electronic systems.

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